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(19)

(54) METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

(71) We, HITACHI LTD., of 1—5—1 Marunouchi, Chiyoda-ku, Tokyo, 100, Japan, a Japanese Company,

do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a method of manufacturing a semiconductor device, especially a silicon gate MOS-type semiconductor device, and to the devices made by the method.

In general, in a semiconductor device having an insulated gate, such as a MOS-field-effect transistor (MOSFET), there is a very thin SiO_2 (silicon dioxide) film constituting an insulating portion. For this reason, even an extremely slight voltage generated in the gate is liable to cause dielectric breakdown of the gate. As a counter-measure, the gate has been protected by arranging a surface breakdown diode in parallel with the gate or by employing a series resistance. In a silicon gate MOS field-effect transistor which uses polycrystalline silicon for the gate, a similar measure against gate destruction has hitherto been taken. It has been shown, however, that the gate is not satisfactorily protected by such a method. In more detail, in the manufacture of the Si gate MOSFET, an SiO_2 film on source and drain regions is selectively etched using the Si gate as a mask. When forming the Si gate, as illustrated in Fig. 1(a) of the accompanying drawings, a polycrystalline Si layer 4a is first photoetched, and an underlying gate SiO_2 layer 3a is subsequently etched. The gate SiO_2 layer 3a therefore undergoes side etching, with the result that the overlying polycrystalline Si layer 4a projects in the form of a "pent roof" at the periphery of the gate SiO_2 layer. Under such a "pent roof" (shown at 4b in the figure), it is difficult sufficiently to form an SiO_2 layer 8 by a CVD (chemical vapour deposition) process employed in the succeeding step of manufacture. Impurities are also prone to be concentrated here. Furthermore, since the pent roof 4b has an acute angle at its extremity and the electric field concentration tends to be increased at this part, which is easily broken by a slight external shock or the like. These drawbacks may lead to a short-circuit. It has been shown that, when a pent roof is formed in the Si gate, dielectric breakdown is liable to occur at this part even at a low gate voltage for the reasons stated above. The present inventors have subjected a number of completed Si gate MOSFETs to an experiment in which the Tested items whose gate withstand voltages were lower than a certain standard value were rejected in a voltage screening test. When the test pieces were 200-bit shift registers, the defective percentage was 4 to 5%. Such testing takes time and lowers the yield because of rejects from the test itself, and besides, results in higher cost.

According to the present invention there is provided a method of manufacturing a semiconductor device comprising the steps of:

(a) forming an insulating layer on a semiconductor substrate of a first conductivity type;

(b) forming a conductor or semiconductor layer on a portion of said insulating layer;

(c) etching said insulating layer adjacent at least one edge portion of said conductor or semiconductor layer in a manner such that the part of the insulating layer underlying the said edge portion of the conductor or semiconductor layer is etched to leave said edge portion projecting beyond the part of said insulating layer remaining beneath the conductor or semiconductor layer; and

(d) converting at least said projecting portion of said conductor or semiconductor layer wholly into insulating material;

Preferably said substrate is a silicon substrate, said insulating layer is silicon dioxide, said conductor or semiconductor layer is polycrystalline silicon and said step (d) is carried out by oxidizing the surface of said polycrystalline layer.

After step (d) a further insulating layer may be formed on the structure produced by

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step (*d*) and metal wirings provided through the further layer at the desired locations.

Particular embodiments f the invention will now be described by way of example with reference to the accompanying drawings in which:—

Figs. 1(*a*) and 1(*b*) illustrate the relevant portion of an MOS construction necessary for explanation of the basis of the present invention, Fig. 1(*a*) being a vertical sectional view of the portion in the case of manufacture by the known method described above, while Fig. 1(*b*) is a vertical sectional view of the portion in the case of manufacture by a method within the present invention;

Figs. 2(*a*) to 2(*g*) are sectional views showing various steps of manufacture in an embodiment of the present invention; and

Figs. 3 to 5 are graphs explaining effects obtainable with the present invention, Fig. 3 illustrating the relationship between V_{th} and the oxidation time of the polycrystalline Si layer, and Fig. 4 illustrating the relationship between V_{th} and the thickness of the oxide layer formed on the polycrystalline Si layer and Fig. 5 illustrating the relationship between the decrease of V_{th} and the time taken to form this layer.

In all three graphs the oxidation conditions given are for the oxidation of the polycrystalline Si layer to form the layer 7, while the figure given for Tox is the thickness of the gate oxide layer 3*a*.

Referring firstly to Figs. 2(*a*) to 2(*g*), these show manufacturing steps in a case where the method of the invention is applied to a P-channel Si gate MOSFET. The various steps are as follows:—

Fig. 2(*a*) An n-type silicon substrate 1 having a specific resistance to 5—8Ωcm is prepared. It is heated in an oxidizing atmosphere at approximately 1,200°C to form a first thermal oxidation film or layer 2 in the surface of the substrate to a thicknes of 14,000 A. Subsequently, that part of the thermal oxidation film 2 which corresponds to a source, a drain and a gate region to be formed in removed by a photoetching technique.

Fig. 2(*b*) Oxidation is again carried out in an oxidizing atmosphere at approximately 1,200°C to form a second thermal oxidation film or layer 3 of 1,250—1,300 A thickness on the substrate surface exposed by step of Fig. 2(*a*). The second thermal oxidation film 3 is used subsequently as a gate insulating film 3*a*. Because the threshold voltage V_{th} is lowered by a third thermal oxidation in the step of Fig. 2(*e*) described below, the thickness f the second thermal oxidation film is chosen so as to be greater by 250—300 A than it usually would have been. Selection of greater thickness in this manner, however, is not always necessary. Where it is desired suitably t lower V_{th}, the thickness of the oxide film, the oxidizing atmosphere, the oxidation temperature and/or the oxidation time may be appropriately varied.

Fig. 2(*c*) Using a CVD process, Si produced by thermally decomposing SiH_4 (monosilane) at about 600°C is deposited on the entire surface of the resultant substrate to a thickness of approximately 5,000 A. Thus, a polycrystalline Si layer 4 is formed.

Fig. 2(*d*) The polycrystalline Si layer 4 and the second thermal oxidation film 3 are selectively removed by photoetching to provide windows for forming source and drain regions on opposite sides of the remaining portions of layers 3 and 4. Boron, for example, is subsequently diffused as an acceptor, thereby to form source region 5 and drain region 6 which are p-type diffused layers (8,000 A thick). In this step an Si gate electrode 4*a* made from the polycrystalline Si layer 4 is formed at the same time and an overhanging projection in the form of a "pent roof" 4*b* is created at each peripheral edge part of the Si gate electrode 4*a* because of side etching during the etching of the second thermal oxidation film 3.

Fig. 2(*e*) Thermal oxidation of the surface of the Si gate 4*a* (the third thermal oxidation) is carried out in an oxidizing atmosphere at approximately 940°C. Here, the thermal oxidation is performed, so that, as illustrated on a larger scale in Fig. 1(*b*), the material of the Si layer 4*a* is converted into a thermal oxidation film or layer 7 which is of sufficient depth to extend at least to the layer 3*a*. In other words, the projection or pent roof 4*b* is wholly oxidized. Since, as stated above, the oxidation is conducted at the comparatively low temperature of 940°C, the oxidizing treatment scarcely gives rise to re-diffusion of the source region 5 and the drain region 6, and the threshold voltage V_{th} is not much reduced. As previously explained, this reduction is corrected for beforehand by controlling the thickness of the gate oxide film. Oxide films 7 are also formed in the surfaces of the source 5 and drain 6 during the third thermal oxidation treatment.

Fig. 2(*f*) Using a CVD process, SiO_2 produced by low-temperature oxidation of SiH_4 at about 450°C is deposited over the entire surface. Thus, a covering CVD oxide film 8 approximately 8,000 A thick is formed.

Fig. 2(*g*) Using photoetching, contact holes for the source region 5, drain region 6 and the gate 4*a* (the contact hole for the gate is not shown) are formed in the CVD oxide film 8. Aluminium is evaporated onto the entire surface, and wirings 9 of a predetermined pattern are formed by photoetching.

With the meth d of construction described above, the following effects and results are achieved.

(1) The pent roof 4*b* of the polycrystalline

Si layer is wholly oxidized at step (e). Therefore, even in a case where the material SiO_2 of the oxide film 8 formed by the CVD process is produced in an imperfect state under the pent roof, or where impurities are concentrated on that part, it never happens that the gate voltage is applied directly to the pent roof. Consequently, the gate portion does not become the reason for the dielectric breakdown from this cause. Moreover, the extremity of the gate portion 4a i.e. the electrically conductive part in the final product, is not acute angled, so that excessive electric field concentration does not tend to occur. Even if the extremity of the gate portion 4a is broken due to any external force, dielectric breakdown is unlikely to arise owing to the presence of the oxide film.

(2) For the reasons set out in the preceding paragraph (1) the gate destruction decreases, and the percentage of devices found defective in the voltage screening process can be brought below 0.1%. In consequence, the necessity for performing the voltage screening process may be eliminated, and it can be omitted.

(3) The polycrystalline Si layer of the gate electrode 4a is surrounded by thermal oxidation films of fine structure. Therefore, when compared with the construction, as in the priort art, in which only the comparatively porous SiO_2 produced by the CVD process exists around the polycrystalline Si, the construction of the present device can remarkably reduce the risk of generation of a short-circuit between a polycrystalline Si wiring (namely, an Si wiring continuous to the gate) and the Al wiring formed over the gate through the CVD oxide film 8.

(4) As illustrated in Figs. 3 to 5 by tests on various embodiments, it is apparent that, as the depth of the surface oxidation of the pent roof portion of the polycrystalline Si layer of the gate electrode is increased, the threshold voltage V_{th} is lowered. The changes in V_{th} vary in dependence on the oxidation time of the polycrystalline Si layer, the thickness of the gate oxide film 3a i.e. the second oxidation layer, the state of the atmosphere and the oxidation temperature for the polycrystalline Si layer. V_{th} can be controlled to a desired value by appropriately combining and controlling the conditions. As shown by the curves in Figs. 3 to 5, a P-channel MOS structure of the depletion mode with a desired characteristic can be produced by selecting the thickness of the oxide film or the length of the oxidation period at an appropriate value.

The foregoing embodiment can, within the scope of the present invention be varied, for example, in the following ways.

(1) For the gate electrode, there may be employed another substance which can be converted into an insulator by oxidation such as molybdenum or tungsten.

(2) For the gate insulating portion, silicon nitride (Si_3N_4) or a multi-layer film of, for example, a lamination of SiO_2 and Si_3N_4 can be used in place of SiO_2.

(3) The MOS construction can be other than that of the MOSFET.

The present invention is applicable to any semiconductor device having an insulated gate, the manufacture of the device including the step of etching an insulating portion by employing a conductor portion as a mask. That is, it is applicable to all sorts of MOS structures of self-alignment construction, for example, to Si gate MOSFET's, Al MOSFET's and MOS IC's including them as constituent elements.

As described above, it is possible by the method within the present invention to diminish the rate of destruction of gates in semiconductor devices of the MOS construction belonging broadly to MIS construction; the defective proportion of semiconductor products of the MIS construction under voltage screening can be reduced for example, below 0.1% for 200-bit shift registers, finally rendering the voltage screening test unnecessary; a gate electrode as well as an interconnection layer made of polycrystalline silicon and an interconnection layer made of aluminium in a silicon gate MOSFET can be protected from short-circuits between them; and the conditions of oxidation of the "pent roof" of a silicon gate in a silicon gate MOSFET may be varied in order to adjust the threshold voltage V_{th} of the device to a desired value.

WHAT WE CLAIM IS:—

1. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming an insulating layer on a semiconductor substrate of a first conductivity type;

(b) forming a conductor or semiconductor layer on a portion of said insulating layer;

(c) etching said insulating layer adjacent at least one edge portion of said conductor or semiconductor layer in a manner such that the part of the insulating layer underlying the said edge portion of the conductor or semiconductor layer is etched to leave said edge portion projecting beyond the part of said insulating layer remaining beneath the conductor or semiconductor layer; and

(d) converting at least said projecting portion of said conductor or semiconductor layer wholly into insulating material.

2. A method according to claim 1 including prior to step (d) the step of

(e) introducing impurities of a second conductivity type into a region of said substrate n at least one side of the structure constituted by the conductor r semiconductor

layer and the said remaining portion of the insulating layer to form a semiconductor region of said second conductivity type in said substrate.

3. The method according to claim 1 r claim 2 further including the steps of (f) forming a further insulating layer covering the structure resulting from step (d); and (g) providing wiring contact layers through said further insulating layer at preselected portions thereof.

4. A method according to claim 2 further including the steps of (f) forming a further insulating layer covering the structure resulting from step (d); and

(g) providing wiring electrode layers through said further insulating layer at predetermined portions thereof to contact said conductor or semiconductor layer and said semiconductor region.

5. A method according to any one of claims 1 to 4 wherein said conductor layer is of polycrystalline silicon, molybdenum or tungsten.

6. A method according to any one of claims 1 to 5 wherein said insulating layer is of silicon dioxide, silicon nitride, or is a multi-layer laminated film of silicon dioxide and silicon nitride.

7. A method according to any one of the preceding claims wherein said substrate is a silicon substrate, said insulating layer is silicon dioxide, said conductor or semiconductor layer is polycrystalline silicon and said step (d) is carried out by oxidizing the surface of said polycrystalline layer.

8. A method according to claim 4 wherein said oxidizing step (e) is carried out at a temperature of about 940°C.

9. A method according to claim 1 substantially as any herein described with reference to Fig. 1 and Fig. 2 of the accompanying drawings.

10. A semiconductor device whenever produced by a method according to any one of the preceding claims.

11. A semiconductor device substantially as any herein described with reference to and as shown in Fig. 2g of the accompanying drawings.

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FIG. 1a

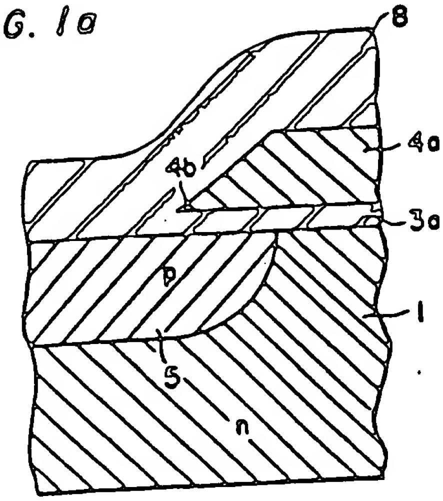


FIG. 1b

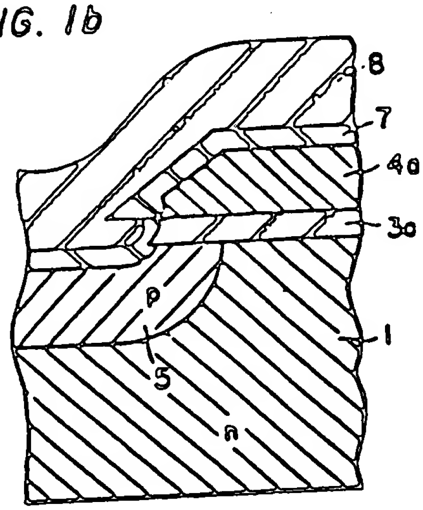


FIG. 2a

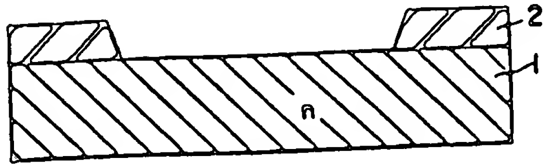


FIG. 2b

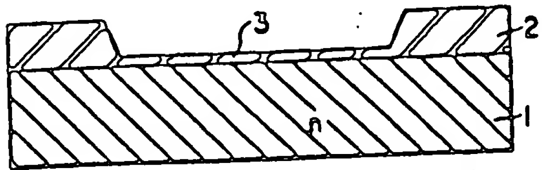


FIG. 2c

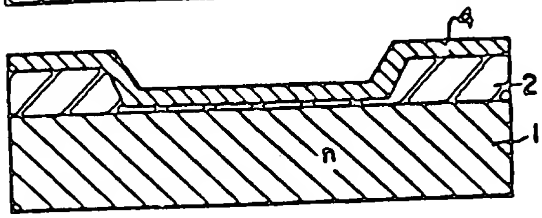


FIG. 2d

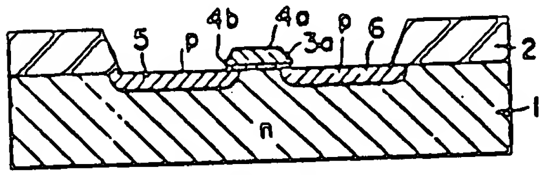


FIG. 2e

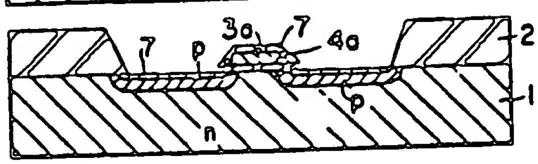


FIG. 2f

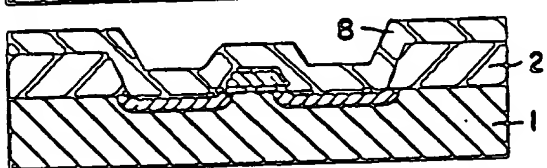


FIG. 2g

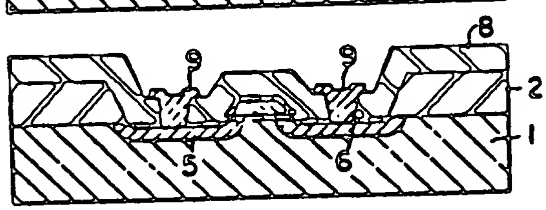
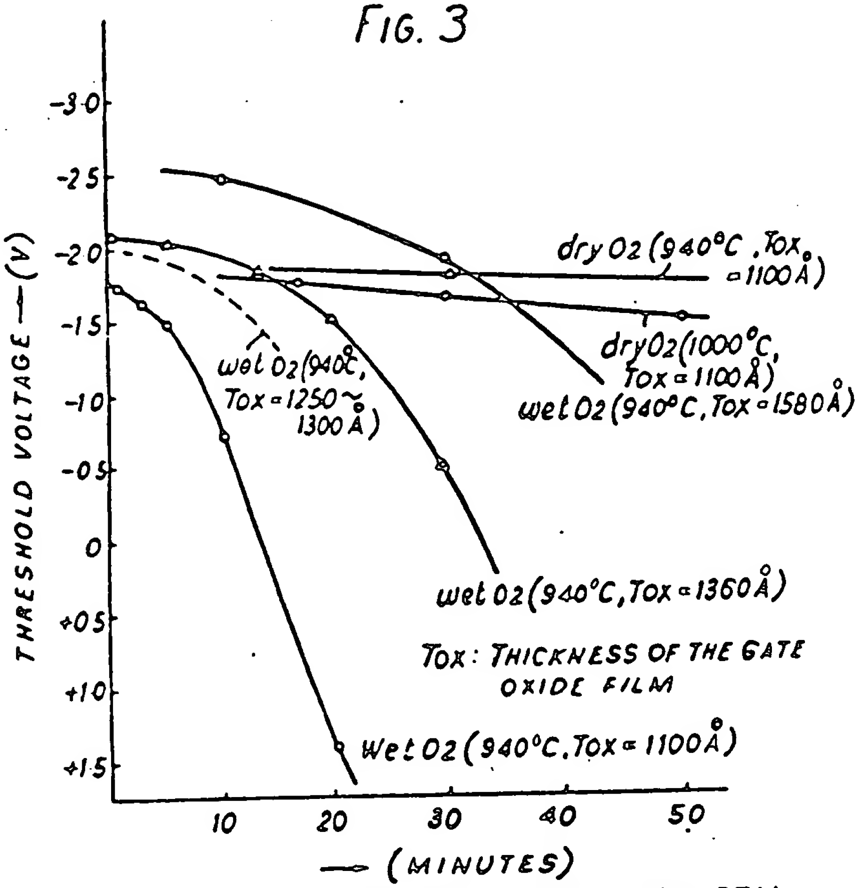
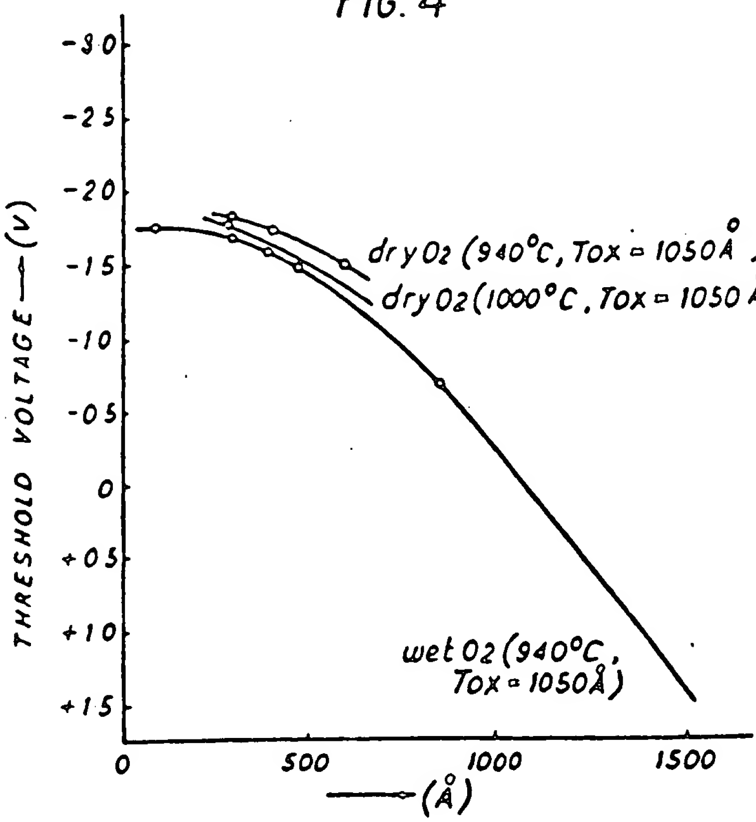


FIG. 3



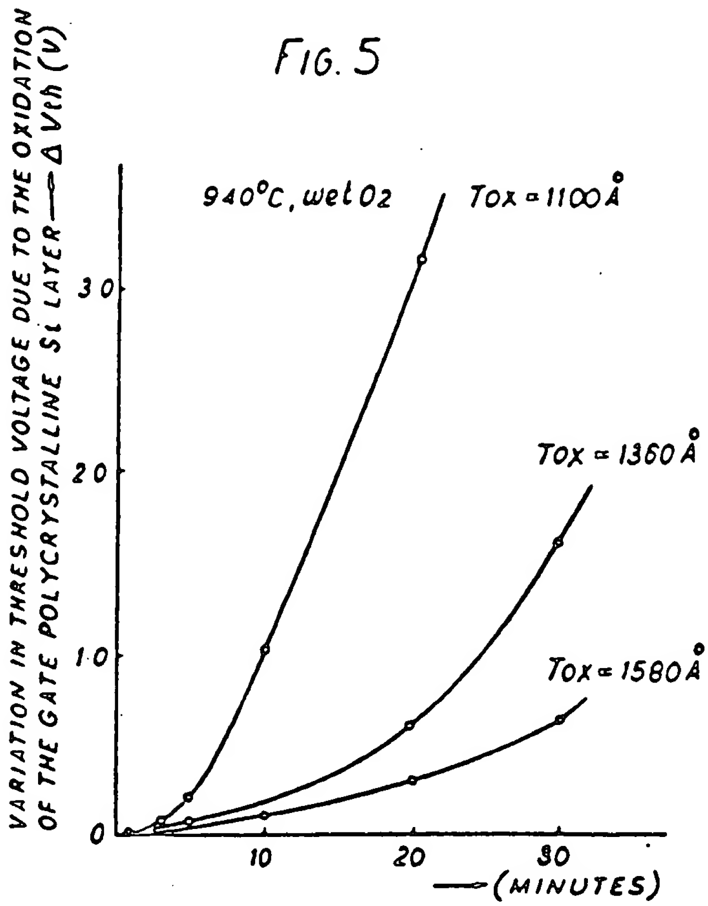
TIME OF OXIDATION OF THE POLYCRYSTAL-LINE Si LAYER

FIG. 4



THICKNESS OF THE OXIDE FILM FORMED BY OXIDATION OF THE POLYCRYSTAL LINE Si LAYER

FIG. 5



TIME OF OXIDATION OF THE POLYCRYSTALLINE Si LAYER